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Description

[METHOD OF CORRECTING LITHOGRAPHIC PROCESS AND METHOD OF FORMING OVERLAY MARK]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 93107051, filed March 17, 2004.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a method of correcting processing errors and a method of forming overlay mark. More particularly, the present invention relates to a method of correcting lithographic process and a method of forming overlay mark capable of preventing errors in alignment measurement when the overlay mark is used for alignment in semiconductor fabrication.

[0004] Description of the Related Art

[0005] In general, aside from a proper control of the critical di-

mension, the yield of a wafer after a photolithograhic operation also depends on alignment accuracy. Therefore, the measurement of alignment accuracy or overlay error measurement in semiconductor fabrication is very important. An overlay mark is an auxiliary tool for measuring overlay errors. The overlay mark is a means of determining if a patterned photoresist layer produced after a photolithographic process is accurately aligned with a previous film pattern. Particularly, after an aluminum conductive line layer has been globally deposited over a wafer and the aluminum layer etched using a photoresist layer in the fabrication of metallic interconnect, the positions of alignment marks and overlay marks are often measured and compared. This ensures the aluminum lines are accurately aligned with the contact or plug. Furthermore, if there is any shifting in the alignment, the next photoresist layer for defining another aluminum line layer can be modified to compensate for the error.

[0006] Typically, the overlay mark is designed to dispose on the corner or peripheral region of chips on the wafer and are formed during the process of forming the metallic interconnects. Hence, if there is some error in the process of fabricating the metallic interconnects, relative positions of

the overlay marks on the wafer will also be affected. In other words, the measured values of various overlay marks will differ.

[0007] As an example, aluminum lines are formed in a sputtering process. During the sputtering process, plasma production is closely related to the production of gaseous plasma ions (for example, argon ions). In other words, the probability of bombardment between high-energy electron and gaseous plasma atoms directly affects the sputtering process. To increase the probability of ionization of the gaseous plasma atoms (the so-called sputtering yield), the mean free path of the electrons within the plasma is preferably increased. At present, the most commonly used method for increasing the mean free path is to deploy an additional magnetron device. Typically, this means that a rotatable magnetron device is installed over a target within a plasma reaction chamber. Thus, through the magnetic field created by the magnetron device, charge particles within the reaction chamber are activated to follow a spiraling motion, thereby increasing the probability of collision. Because electrons are light particles, they have a very small radius of gyration and are mostly constrained to move within a short distance from the mag-

netic lines. In other words, electrons will mostly spiral near the magnetic field and increase the plasma ion density as well as ion bombardment frequency there.

[0008] Because the magnet above the target rotates around a center, the bombarded surface of the target will develop concentric openings after a period of time. Since the target surface is no longer a flat surface, a portion of the sputtered metallic atoms may collide with the sidewalls of the openings and lead to a change in the sputtering rate between the central and peripheral portion of the target. When the sputtered atoms reach the recess hole or openings on the wafer, the sidewalls facing the central direction and the peripheral direction of the target will have different sputtered film thickness. Moreover, as the sputtering operation is continued, the amount of variation in the concentric opening will increase and the magnetic field strength at the sputtering location will intensify. Ultimately, asymmetric deposition of the sputtered film is amplified as shown in Figs. 1A and 1B.

[0009] In the meantime, gaseous plasma ions subjected to the magnetic field from the magnetron device will bombard the target surface at a small biased angle so that quantity of sputtered metallic atoms in the reflecting direction is

larger than in the other direction. The asymmetrical deposition caused by the magnetic lines parallel to the direction of rotation that activates the gaseous plasma ions to follow a direction perpendicular to the direction of rotation is neutralized by the rotation of the magnetron device. However, the magnetic lines perpendicular to the direction of rotation lead to an asymmetric deposition in a direction parallel to the direction of rotation. Figs. 1A and 1B are diagrams showing a thin film on an opening section within a lithographic mark or overlay mark on a wafer using a conventional D.C. magnetron sputtering method. Due to the presence of concentric openings on the target and the effect of the magnetic lines on the sputtering angle of gaseous plasma ions relative to the bombarding target, the film 102 on the wafer 100 may be asymmetrically deposited on the sidewalls of the openings 104. Consequently, there will be a rotational shift (labeled 106) or radial shift (labeled 108) in the coordinates of the overlay mark.

[0010] In general, overlay mark measurement is based on the height difference on the surface of a wafer as measured by the difference in brightness at various interfaces. When a metallic film on the sidewall of an opening is asymmet-

rically deposited, the mid-point obtained by gauging the height difference of opening sidewalls may deviate from the true value. Furthermore, the degree of asymmetrical deposition will increase in proportional to the target consumption and hence the degree of shifting will increase with use. Although the shifting problem in lithographic process can be rectified through a few adjusting steps, this is not an efficient means because each depositing station and the circumstance around each shifting event are different.

SUMMARY OF INVENTION

[0011] Accordingly, The present invention is directed to a method of correcting a lithographic process capable of reducing the problem of an increase in asymmetrical deposition of a thin film with the degree of target consumption in a physical vapor deposition (PVD) process, and thereby reducing a change in the degree of shifting in a subsequently deposited metallic conductive lines relative to the overlay mark of a previous pattern.

[0012] The present invention is directed to a method of forming an overlay mark capable of reducing the problem of a shift in the overlay mark due to a thin film deposition using a conventional PVD process, and thereby reducing an

error in measuring the overlay mark.

[0013] The present invention is directed to a method of correcting a lithographic process capable of reducing the problem of an increase in the degree of shifting in the overlay mark with processing frequency, and thereby reducing an error in measuring the overlay mark.

[0014] According to an embodiment of the present invention, a method of correcting a lithographic process provided. First, a physical vapor deposition process (PVD) is performed to deposit a film on a wafer. The deposited film leads to a shift in the overlay mark and the degree of shifting in the overlay mark is related to the target consumption in the PVD process. A formula relating the target consumption and the degree of shifting can be derived. The formula is stored inside a controller system. A compensation value can be obtained from the controller system through a computation based on the target consumption/overlay mark shifting formula. The compensation value can be fed back in a subsequent lithographic process. Thereafter, a photoresist layer is formed on the film and a lithographic process is performed to pattern the photoresist. During the lithographic process, the controller system feeds back the compensation value to cor-

rect the positional shift resulting from target consumption in the PVD process. In the aforementioned process of computing a compensation value, either a corresponding compensation value is obtained for each wafer or a corresponding compensation value is obtained for each batch having a specified number of wafers.

[0015] The present invention also directed to a method of forming an overlay mark. The method is suitable for forming the overlay mark over a wafer having a material layer thereon. First, an opening pattern is formed in the material layer to serve as an outer mark. Thereafter, a first film layer is formed over the material layer. A portion of the first film is removed to expose a portion of the material layer. A physical vapor deposition (PVD) process is carried out to form a second film layer over material layer covering the first film layer. The deposited second film layer has a certain degree of shifting according to the target consumption in the PVD process. A formula can be found within the degree of shifting with the target consumption. The formula is recorded by a controller system. Hence, the controller system is able to compute a compensation value and feeds the compensation value back in a subsequent lithographic process. Thereafter, a photoresist layer

is formed on the second film layer and a lithographic process is performed to pattern the photoresist into an inner mark. During the lithographic process, the controller system feeds back the compensation value to correct for the positional shift resulting from target consumption in the PVD process. In the aforementioned process of computing a compensation value, either a corresponding compensation value is obtained for each wafer or a corresponding compensation value is obtained for each batch having a specified number of wafers.

[0016] The present invention is also directed to a method of correcting a lithographic process. First, a physical vapor deposition (PVD) process is carried out to form a thin film layer over a wafer. The deposited thin film will lead to a shift in the overlay mark on the film layer. The degree of shifting in the overlay mark is related to the target consumption in the PVD process. A formula can be found within the degree of shifting with the target consumption. Thereafter, a first compensation value is obtained through the formula. A photoresist layer is formed over the film layer. The first compensation value is combined with a set of data for correcting a lithographic process to produce a second compensation value. A lithographic process is

performed to pattern the photoresist layer. During the lithographic process, the second compensation value is feed back to correct for the positional shift resulting from target consumption in the PVD process.

[0017] According to an embodiment of the present invention, a compensation value is fed back to correct the different amount of shifting in the overlay mark on a wafer due to physical vapor deposition or some other processes. Therefore, error in measuring the position of the overlay mark due to a shift in the overlay mark can be reduced. In other words, the problem of having a misalignment between a patterned film layer and a previous film layer can be reduced. Furthermore, the method of correcting a lithographic process through a formula that relates the target consumption in the PVD process with the degree of shifting in the overlay mark can be used together with other methods of correcting the lithographic process.

[0018] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0019] The accompanying drawings are included to provide a

further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0020] Figs. 1A and 1B are diagrams showing a thin film on a opening section within a lithographic mark or overlay mark on a wafer using a conventional D.C. magnetron sputtering method.

[0021] Fig. 2 is a top view of an overlay mark used in a conventional fabrication process of metallic interconnect.

[0022] Figs. 3A through 3F are schematic cross-sectional views showing the steps for fabricating an overlay mark according to one embodiment of the present invention.

[0023] Fig. 4 is a flow diagram showing the steps for correcting a lithographic process according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0024] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like

parts.

[0025] According to an embodiment of the present invention, a method of correcting a lithographic process and a method of forming an overlay mark is provided. A compensation value according to a relationship between the target consumption in a physical vapor deposition (PVD) process and degree of shifting in the overlay mark is computed and then fed back to correct the parameters used in a lithographic process. Hence, misalignment between the lithographic process and a previous film layer on the wafer due to an error in measuring the alignment of the overlay mark can be reduced. In the following, the steps for forming an overlay mark in the fabrication of metallic interconnect are illustrated as an example. However, the usefulness of the present invention is not limited to the fabrication of metallic interconnect. In addition, although the method of correcting a lithographic process is illustrated using a relationship between the degree of shifting and the target consumption in a physical vapor deposition (PVD) process, the present invention is not limited as such. The present invention can be applied to other processes that involve a definite relationship between the degree of shifting and the frequency of the processing oper-

ation.

[0026] Fig. 2 is a top view of an overlay mark used in the fabrication process of metallic interconnect. Figs. 3A through 3F are schematic cross-sectional views showing the steps for fabricating an overlay mark according to one embodiment of the present invention. In fact, Figs. 3A through 3F show a cross-section along line I-I" of Fig. 2. In the process of fabricating a metallic interconnect as shown in Figs. 2 and 3A, a substrate 200 having a chip region and an overlay mark region is provided. A material layer 202 is deposited on the substrate 200. Thereafter, a photolithographic process and an etching process are carried out to pattern the material layer 202 so that a plurality of contact openings (not shown) is formed in the material layer 202 within the chip region. The material layer 202 is fabricated using an insulating material, for example. In the meantime, an opening pattern 204 is formed in the overlay mark region of the substrate 200 to serve as an outer mark. In one embodiment of the present invention, the outer mark of the overlay mark comprises four opening patterns 204 positioned to form a rectangular structure. Furthermore, the opening pattern 204 has a width much greater than the contact opening.

[0027] As shown in Fig. 3B, a metallic material is deposited to form a metallic layer 206 over the material layer 202. The metallic layer 206 fills the contact opening within the chip region and the opening 204 within the overlay mark region. Because the contact opening has a width much smaller than the opening 204, the metallic layer 206 fills the contact opening completely but only partially fills the opening 204.

[0028] As shown in Fig. 3C, a portion of the metallic layer 206 is removed to expose a portion of the material layer 202. The metallic layer 206 can be removed, for example, by performing a chemical-mechanical polishing operation. The metallic layer 206 outside the contact opening within the chip region is removed to form a plug structure (not shown). At the same time, the metallic layer 206 outside the opening 204 within the overlay mark region is also removed to form a metallic layer 206a that only partially fills the opening 204.

[0029] As shown in Fig. 3D, another metallic layer 208 is formed over the dielectric layer 202. Thereafter, the metallic layer 208 within the chip region is patterned to form a conductive line that connects with the contact plug. Within the overlay mark region, the metallic layer 208 on the outer

mark area fills the opening 204 and covers the metallic layer 206a. Because the opening 204 has a sufficiently large width, the metallic layer 208 will not fill the opening 204 completely. Here, the metallic layer 208 is fabricated using a material selected from a group consisting of titanium, cobalt, nickel, tantalum, tungsten, aluminum and copper, for example.

[0030] It should be noted that the metallic layer 208 is formed in a DC magnetron sputtering process. After the target within the sputtering station has been used for some time, concentric openings are formed on the surface of the bombarded target and the angle of incident of the bombarding gaseous plasma ions is affected because of the effect produced by a rotating magnetic field. Therefore, the metallic layer 208 is asymmetrically deposited as shown in Fig. 3D. Ultimately, there is a shift in the overlay mark. Aside from a shift in a direction away from the center of the wafer as shown in Fig. 3D, the deposition may be a radial shift towards the center of the wafer or a rotational shift (106 in Fig. 1A). In addition, the rotational shift (106) can be a clockwise rotation or an anti-clockwise rotation, for example.

[0031] To reduce subsequent errors in measuring the overlay

mark due to an asymmetrical deposition of the metallic layer 208, a series of steps as shown in Fig. 4 aiming to correct the subsequently performed lithographic process is carried out first.

[0032] As shown in Fig. 4, after performing the physical vapor deposition (PVD) process (step 300), a photoresist layer is directly formed (step 304). In other embodiments, after performing the physical vapor deposition (PVD) process (step 300), an anti-reflection coating (ARC) or a hard mask is formed, and then a photoresist layer is formed on the anti-reflection coating (ARC) or the hard mask. Thereafter, a lithographic process is carried out (step 306) to form a patterned photoresist layer for patterning the metallic layer 208. Since the degree of shifting in the deposited film on the wafer depends on the target consumption in the PVD process (step 300), a formula can be found relating the two. In the present invention, a compensation value is obtained using the aforementioned formula after the PVD process (step 300). After forming the photoresist layer (step 304), the lithographic process (step 306) is carried out, taking into account the feedback compensation value.

[0033] The aforementioned formula is recorded within a control

system. The control system computes a compensation value based on the target consumption and the formula and feeds back the value before carrying out the lithographic process. The control system is an advanced process control (APC) system, for example. In addition, the formula may be obtained by performing a statistical analysis between all the previously recorded target consumption of the PVD target and the corresponding shift. Moreover, there is no particular restriction on the unit for measuring target consumption. For example, the target consumption can be in kilowatt·hour. It should be noted that the control system might also record the target consumption of each PVD process and its corresponding shift (to obtain new data point) so that the target consumption versus shift formula can be renewed from time to time.

[0034] As shown in Figs. 3E and 4, a photoresist layer 211 is formed over the metallic layer 208 (step 304). The photoresist layer 211 is formed, for example, by performing a spin coating and a thermal baking process.

[0035] As shown in Figs. 2, 3F and 4, a lithographic process of the photoresist layer 211 is carried out (step 306) to form a patterned photoresist layer over the metallic layer 208 within the chip region. In the meantime, an overlay mark

pattern 212 is also formed on the metallic layer 208 within the overlay mark region to serve as an inner mark. During the lithographic process (step 306), the control system feeds back the previously computed compensation value to correct any error in the alignment and exposure step.

[0036] After the lithographic process, a measurement of the overlay mark is carried out. As shown in Fig. 3F, the dash line 201 located at the central point signal between two corner regions (arrow indicated) of the metallic layer 208 above the outer mark 204. Similarly, the dash line 203 located at the central point signal between two edge regions (arrow indicated) of the inner mark 212. The locations of the inner mark 214 and central point signal 205 for a lithographic process are carried out without feeding any compensation value are also displayed.

[0037] In the conventional technique, the signal 201 of the outer mark 204 and the signal 205 of the inner mark 214 are used to determine whether the inner mark is accurately aligned with the outer mark. Here, the outer mark represents the overlay mark of the previous pattern and the inner mark represents the current layer or the overlay mark on the metallic layer. In theory, the shift between the cur-

rent layer and the previous pattern can be found by comparing the distance between the central point of the outer mark and the central point of the inner mark. However, the signal 204 is produced not from the central point, nor is there any compensating correction for the signal 205. Although the inner mark 214 and the outer mark 204 are aligned according to distances A and A', the lithographic process has already produced some shift. Hence, if the photoresist layer is subsequently used to define the metallic layer 208, the contact opening will not align accurately with the conductive line.

[0038] In the present invention, the inner mark/outer mark alignment and hence the alignment accuracy of the lithographic process in the present invention cannot be determined by the signal 201 of the inner mark 204 and the signal 203 of the outer mark 212 as in the conventional technique (for example, the value of B and B"). However, adjusting the position of the inner mark 212 directly through the compensation value to correct for any shifting produced after the PVD process, alignment accuracy of the lithographic process is reconstituted. For example, if the deposition shifts towards the direction 210, the compensation value adjusts the position of the inner mark

212 towards the direction 216. Therefore, aside from a change in the position of the inner mark 212 due to the feedback compensation value, the location of the patterned photoresist within the chip region will be adjusted correspondingly. In other words, the method of using a compensation value to correct for any positional shift after a PVD process is an effective means of resolving erroneous overlay mark measurement that results from a shift in the overlay mark position.

[0039] It should be noted that a compensation value could be obtained for each wafer in step 302. Obviously, it is equally feasible to obtain a compensation value for a batch of wafers with each batch comprising a definite number wafers. Furthermore, after a particular compensation value has been used for some time, the controller system may produce a new compensation value using the same target consumption/shifting formula. Alternatively, a new statistical analysis may be performed using the newly obtained target consumption/shifting data to produce a new formula before computing a new compensation value for a subsequent lithographic process.

[0040] In another embodiment of the present invention, after using the formula of PVD target consumption and the shift

to obtain a first compensation value (step 302) for one particular shift value, the first compensation value and other data of a lithographic system may be combined together to produce another compensation value (a second compensation value) as shown in step 308 in Fig. 4. Thereafter, a lithographic process is carried out (step 306). The other lithographic system may include, for example, a station for exposing photoresist. Thus, before carrying out the lithographic process (step 306), a number of corrections aiming at one/batch of the lithographic processes can be carried out to improve overall accuracy.

[0041] In summary, major advantages of the present invention at least includes:

[0042] 1. The present invention utilizes the feedback of a compensation value to correct the positional shift of overlay mark that results from a PVD or other process. Therefore, erroneous measurement of the overlay mark leading to the misalignment between the patterned film layer and the previous film layer is reduced. Furthermore, the method of using the relationship between PVD target consumption and the shift for correcting a lithographic process can be combined with any other correction methods.

[0043] 2. In addition to providing a compensation value, the con-

trol system that hold the formula of the target consumption and the shift may record target consumption of each PVD process and its corresponding shift (fresh new data points can be collected in operation). Thus, the formula of the target consumption and the shift can be renewed from time to time.

[0044] 3. When the method of the present invention is used to pattern metallic conductive lines, the conductive lines can be aligned more accurately. Furthermore, unlike the conventional method, there is no need to adjust the compensation value each time the alignment mark or the overlay mark is shifted. Hence, processing operation is simplified.

[0045] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.